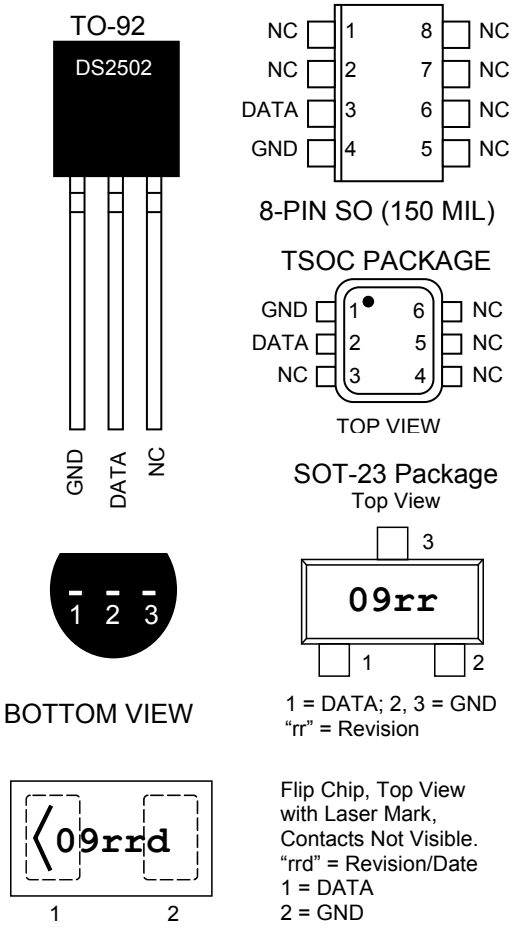
DS2502
1Kb Add-Only Memory

FEATURES

- 1024 bits Electrically Programmable Read Only Memory (EPROM) communicates with the economy of one signal plus ground
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- EPROM partitioned into four 256-bit pages for randomly accessing packetized data
- Each memory page can be permanently write-protected to prevent tampering
- Device is an “add only” memory where additional data can be programmed into EPROM without disturbing existing data
- Architecture allows software to patch data by superseding an old page in favor of a newly programmed page
- Reduces control, address, data, power, and programming signals to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3 kbits per second
- 8-bit family code specifies DS2502 communications requirements to reader
- Presence detector acknowledges when the reader first applies voltage
- Low cost TO-92 or 8-pin SO, SOT-23 (3-pin), TSOC and flip chip surface mount package
- Reads over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C; programs at 11.5V to 12.0V from -40°C to +50°C

PIN ASSIGNMENT



See 56-G7010-001 for package outline.

NOTE: The leads of TO-92 packages on tape-and-reel are formed to approximately 100 mil (2.54 mm) spacing. For details refer to drawing 56-G0006-003.

ORDERING INFORMATION

Standard	Lead-Free	Description
DS2502	DS2502+	TO-92 Package
DS2502/T&R	DS2502+T&R	TO-92 Package, 2k Tape & Reel
DS2502R/T&R	DS2502R+T&R	3-pin SOT-23 Package, 3k Tape & Reel
DS2502P	DS2502P+	6-pin TSOC Package
DS2502P/T&R	DS2502P+T&R	TSOC Package, 4k Tape & Reel
DS2502S	DS2502S+	8-pin SO Package
DS2502S/T&R	DS2502S+T&R	SO Package, 2.5k Tape & Reel
DS2502X1		Flip Chip, 10k Tape & Reel

+ Indicates lead-free compliance.

DESCRIPTION

The DS2502 1Kb Add-Only Memory identifies and stores relevant information about the product to which it is associated. This lot- or product-specific information can be accessed with minimal interface-for example, a single port pin of a microcontroller. The DS2502 consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (09h) plus 1Kb of EPROM which is user-programmable. The power to program and read the DS2502 is derived entirely from the 1-Wire® communication line.

Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The entire device can be programmed and then write-protected if desired. Alternatively, the part may be programmed multiple times with new data being appended to, but not overwriting, existing data with each subsequent programming of the device. Note: Individual bits can be changed only from a logical 1 to a logical 0, never from a logical 0 to a logical 1. A provision is also included for indicating that a certain page or pages of data are no longer valid and have been replaced with new or updated data that is now residing at an alternate page address. This page address redirection allows software to patch data and enhance the flexibility of the device as a stand-alone database. The 48-bit serial number that is factory-lasered into each DS2502 provides a guaranteed unique identity which allows for absolute traceability. The familiar TO-92 or SOIC or TSOC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, maintenance records, asset tracking, product revision status, and access codes.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2502. The DS2502 has three main data components: 1) 64-bit lasered ROM, 2) 1024-bit EPROM, and 3) EPROM Status Bytes. The device derives its power for read operations entirely from the 1-Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this “parasite” power source during the low times of the 1-Wire line until it returns high to replenish the parasite (capacitor) supply. During programming, 1-Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The 1-Wire line must be able to provide 12 volts and 10 milliamperes to adequately program the EPROM portions of the part. Whenever programming voltages are present on the 1-Wire line a special high voltage detect circuit within the DS2502 generates an internal logic signal to indicate this condition. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the six ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +12.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 11
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7, 8
Programming Voltage @ 10 mA	V_{PP}	11.5		12.0	V	

CAPACITANCE (t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	
Delay to Program	t_{DP}	5			µs	10
Delay to Verify	t_{DV}	5			µs	10
Program Pulse Width	t_{PP}	480		5000	µs	10, 12
Program Voltage Rise Time	t_{RP}	0.5		5.0	µs	10
Program Voltage Fall Time	t_{FP}	0.5		5.0	µs	10

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pullup voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1-Wire bus.)

6. V_{IH} is a function of the external pullup resistor and the pull-up voltage.

7. 30 nanocoulombs per 72 time slots @ 5.0V.

8. At V_{CC}=5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.

9. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pullup the data line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

10. Maximum 1-Wire voltage for programming parameters is 11.5V to 12.0V; temperature range is -40°C to +50°C.

11. Under certain low-voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.

12. The accumulative duration of the programming pulses for each address must not exceed 5 ms.